

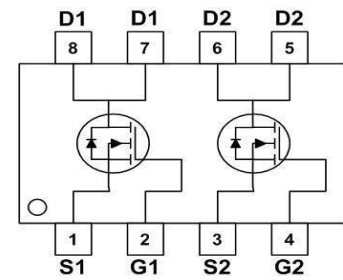


## MXN30D12M

### Dual N-Channel Enhancement Mode Power MOSFET

#### Description

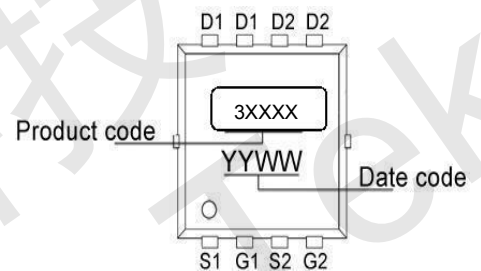
The MXN30D12M uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications



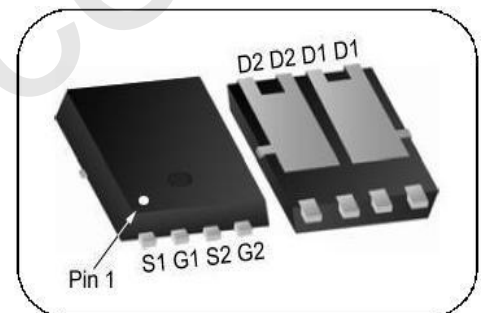
#### General Features

- ◆  $V_{DS} = 30V$ ,  $I_D = 12A$
- ◆ @ $V_{GS} = 4.5V$   $R_{DS(ON)}(Typ.) = 14m\Omega$
- ◆ @ $V_{GS} = 2.5V$   $R_{DS(ON)}(Typ.) = 18m\Omega$
  
- ◆ High density cell design fo ultra low Rdson
- ◆ Fully characterized Avalanche voltage and current

#### Schematic diagram



#### Marking and pin Assignment



PDFN3.3x3.3-8L

#### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	12	A
Drain Current-Continuous( $T_c=70^\circ C$ )	$I_D(70^\circ C)$	9	A
Pulsed Drain Current	$I_{DM}$	48	A
Maximum Power Dissipation	$P_D$	1.7	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$



### Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF Characteristics</b>						
Drain-source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	30	-	-	V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-body leakage	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V	-	-	±100	μA
<b>ON Characteristics</b>						
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	1.2	1.8	2.5	V
Drain-source on-state resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-4A	11	12	14	
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A	14	15.5	18	
Forward transconductance	g <sub>fs</sub>	V <sub>GS</sub> =-5V, I <sub>D</sub> =-4.2A	-	24	-	mΩ
<b>Dynamic Characteristics</b>						
Input capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V f=1.0MHz	-	940	-	pF
Output capacitance	C <sub>OSS</sub>		-	131	-	
Reverse transfer capacitance	C <sub>RSS</sub>		-	109	-	
<b>Switching Characteristics</b>						
Turn-on delay time	t <sub>D(ON)</sub>	V <sub>DD</sub> =-15V I <sub>D</sub> =-4.2A V <sub>GEN</sub> =-10V R <sub>L</sub> =10ohm R <sub>GEN</sub> =6ohm	-	4.2	-	ns
Rise time	t <sub>r</sub>		-	8.2	-	
Turn-off delay time	t <sub>D(OFF)</sub>		-	31	-	
Fall time	t <sub>f</sub>		-	4	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> =-15V, I <sub>D</sub> =-4.2A V <sub>GS</sub> =-4.5V	-	9.63	-	nC
Gate-source charge	Q <sub>gs</sub>		-	3.88	-	
Gate-drain charge	Q <sub>gd</sub>		-	3.44	-	
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A	-	-	1	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	9	A

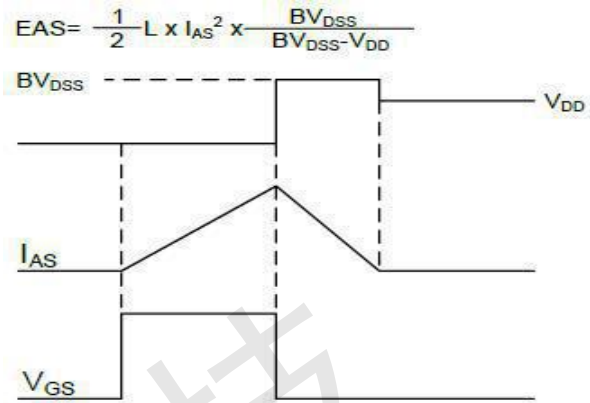
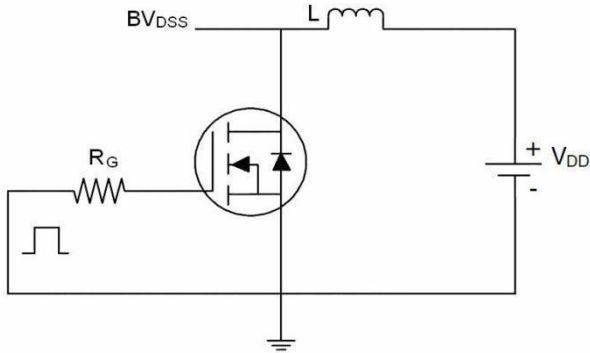
#### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

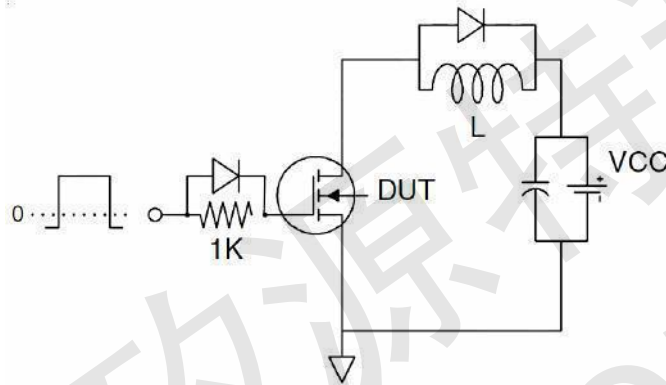


### Test circuit

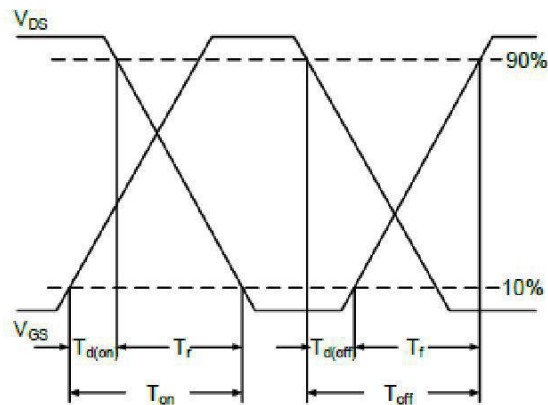
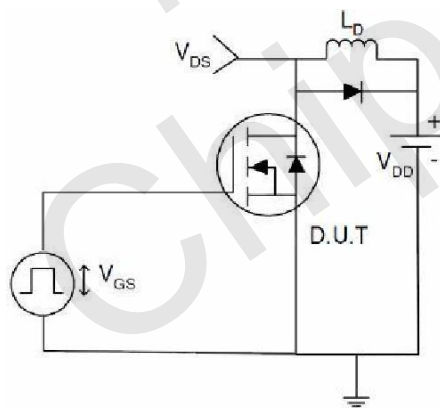
#### 1) EAS test Circuits and waveform:



#### 2) Gate charge test Circuit:



#### 3) Switch Time Test Circuit and waveform





TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

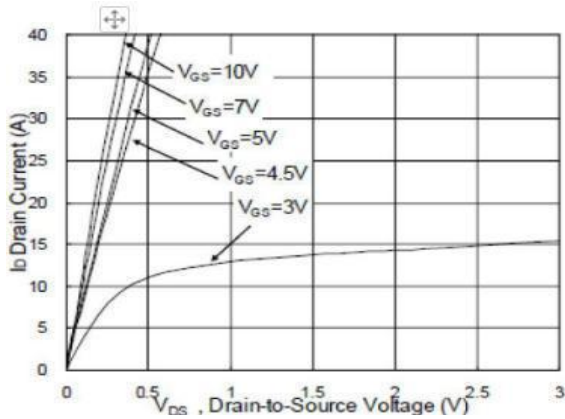


Figure 1 Output Characteristics

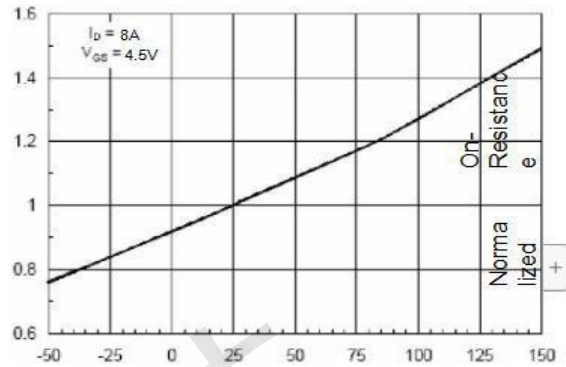


Figure 4 Rdson-Junction Temperature

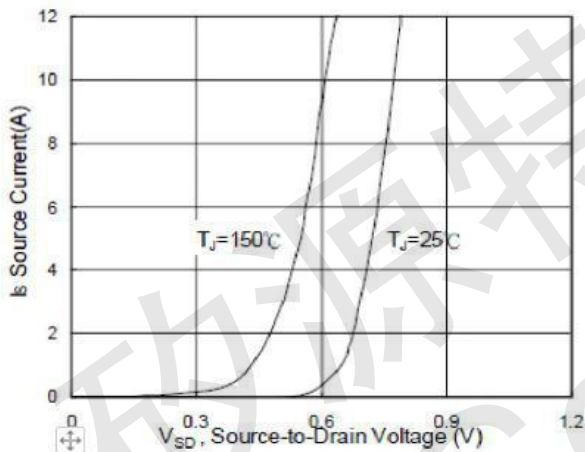


Figure 2 Transfer Characteristics

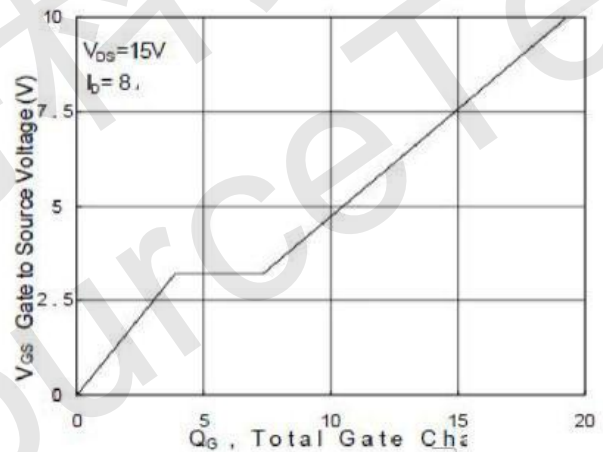


Figure 5 Gate Charge

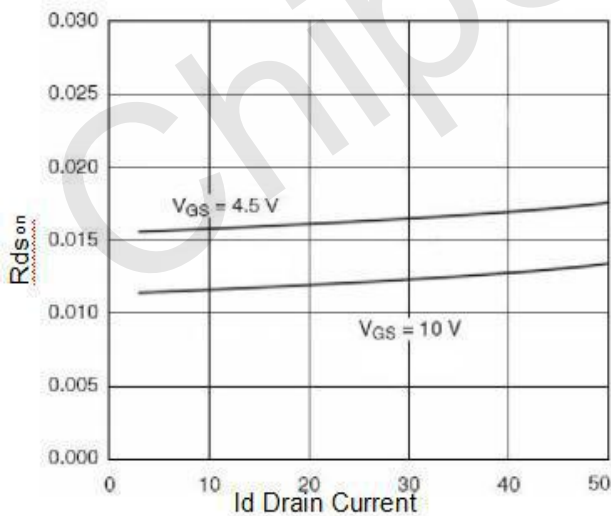


Figure 3 Rdson vs Id

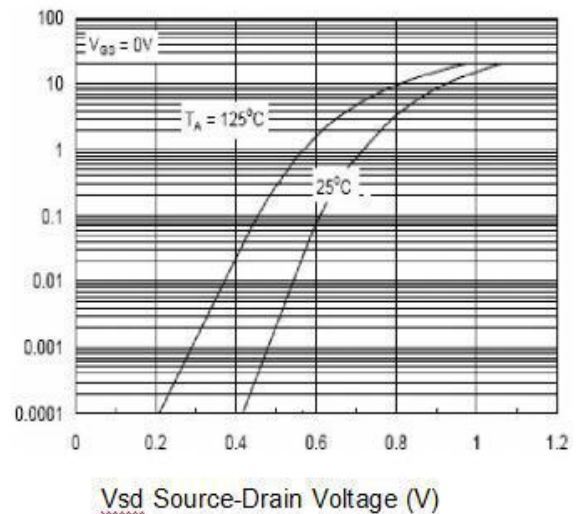


Figure 6 Source- Drain Diode Forward



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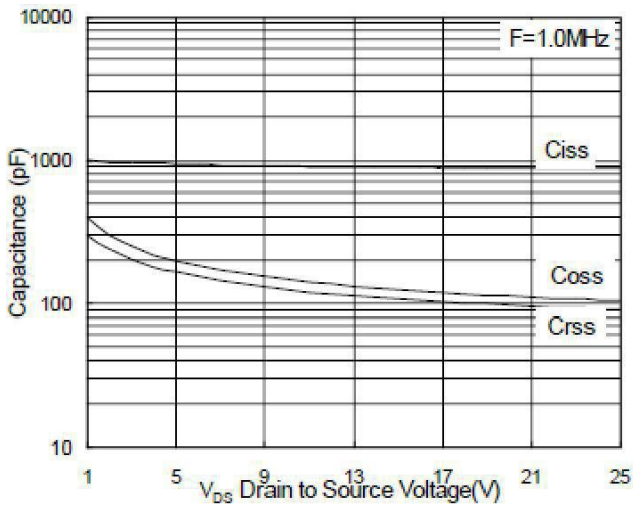


Figure 7 Capacitance vs Vds

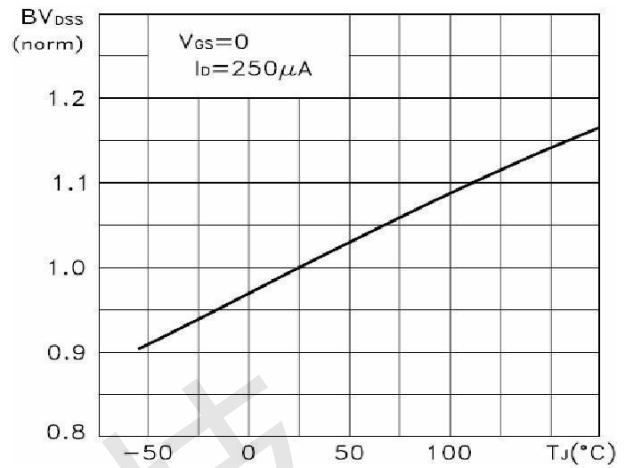


Figure 9 BVdss vs Junction Temperature

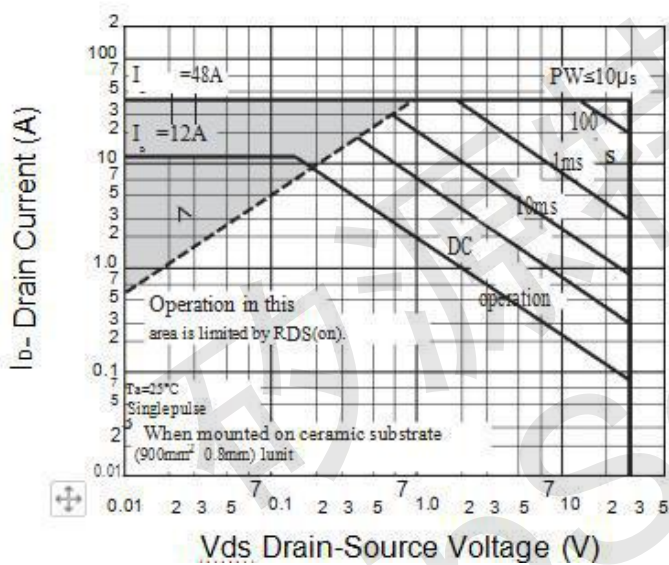


Figure 8 Safe Operation Area

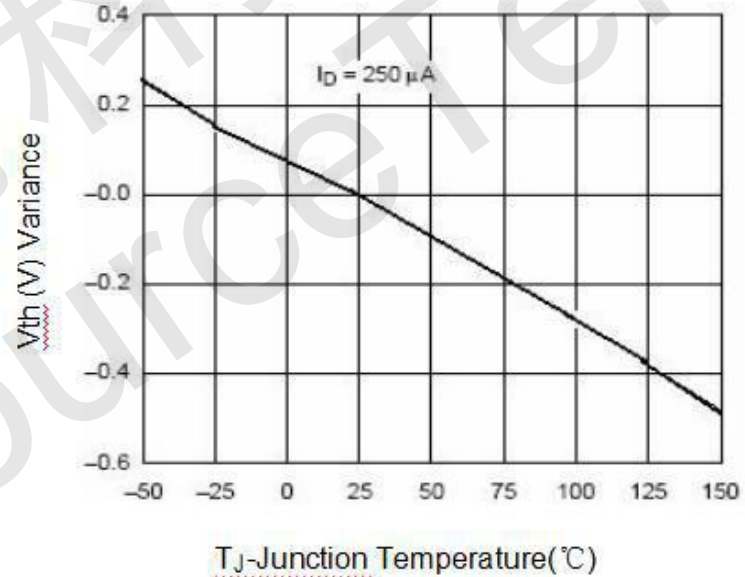


Figure 10 VGS(th) vs Junction Temperature

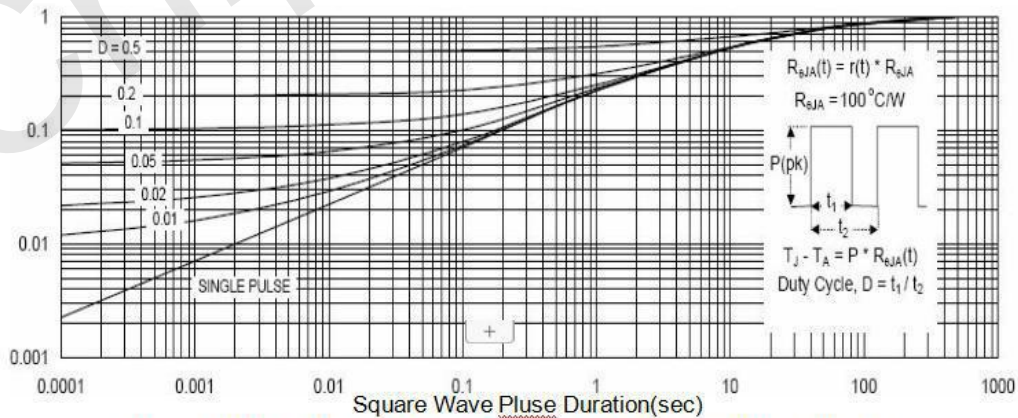


Figure 11 Normalized Maximum Transient Thermal Impedance



**PACKAGE OUTLINE DIMENSIONS**

